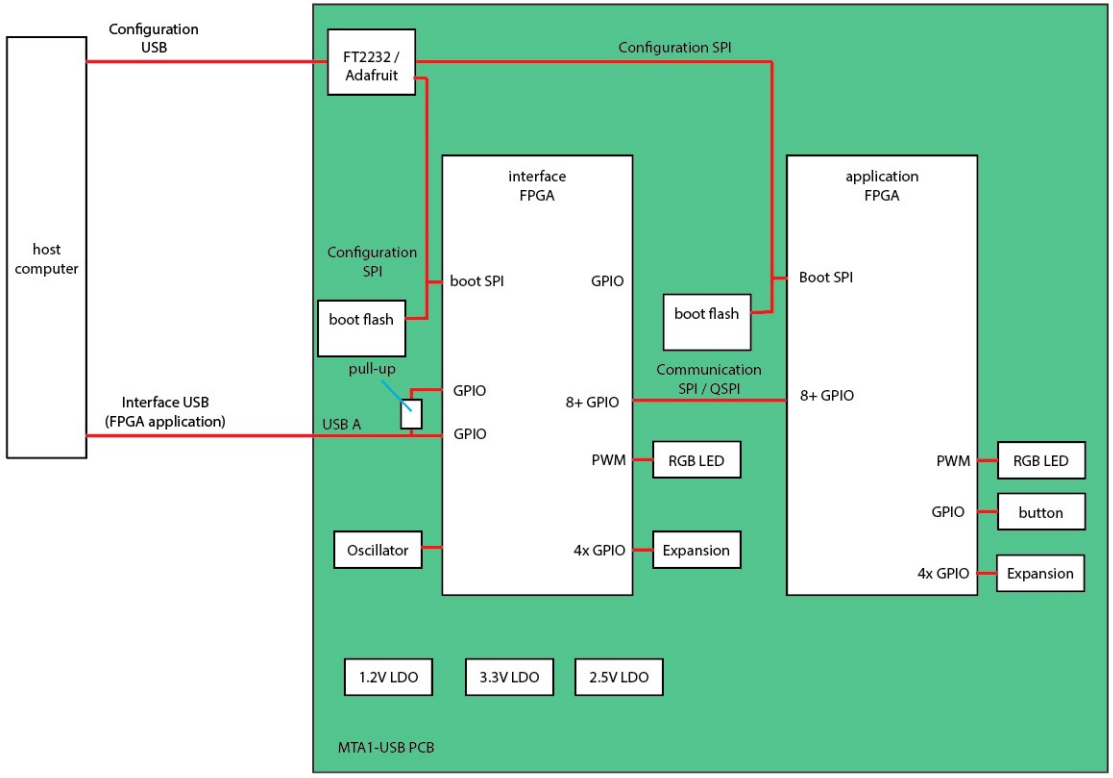


Application FPGA

File: application_fpga.kicad_sch

Interface FPGA

File: interface_fpga.kicad_sch

Power Supply

File: powersupply.kicad_sch

Programming Interface

File: programming_interface.kicad_sch

H1 MountingHole

H2 MountingHole

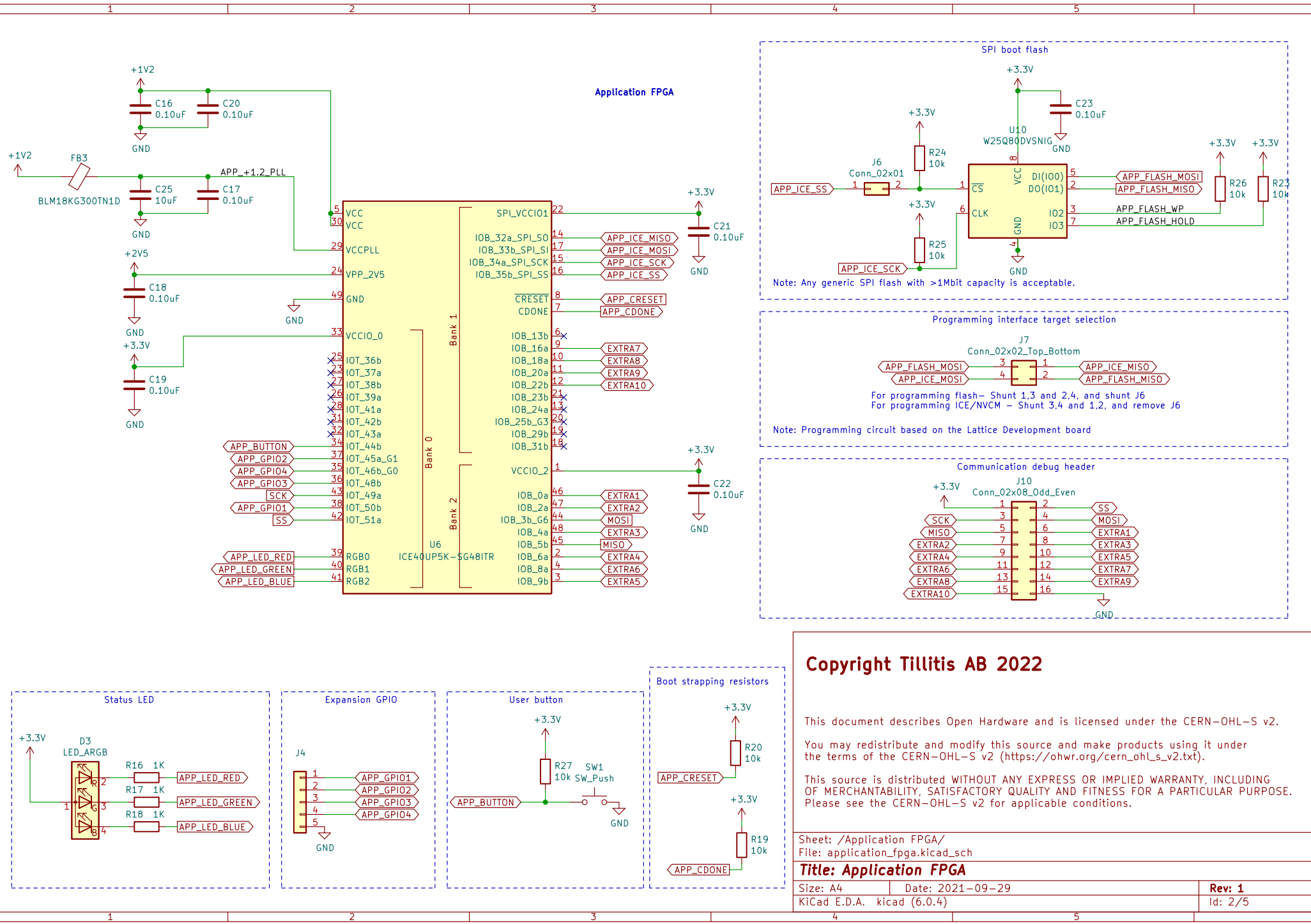
H3 MountingHole

H4 MountingHole

Sheet: /
File: mta1_usb_dev.kicad_sch

Title: MTA1-USB-DEV

Size: A4	Date: 2021-09-29	**Rev: 1**
KiCad E.D.A. kicad (6.0.4)		Id: 1/5


Application FPGA
U6
ICE40UP5K-SG48ITR
Bank 0
Bank 1
Bank 2
SPI boot flash
U10
W25Q80DVSNIG
Note: Any generic SPI flash with >1Mbit capacity is acceptable.
Programming interface target selection
J7
Conn_02x02_Top_Bottom
For programming flash– Shunt 1,3 and 2,4, and shunt J6
For programming ICE/NVCM – Shunt 3,4 and 1,2, and remove J6
Note: Programming circuit based on the Lattice Development board
Communication debug header
J10
Conn_02x08_Odd_Even
Status LED
D3
LED_ARGB
Expansion GPIO
J4
User button
SW1
SW_Push
Boot strapping resistors
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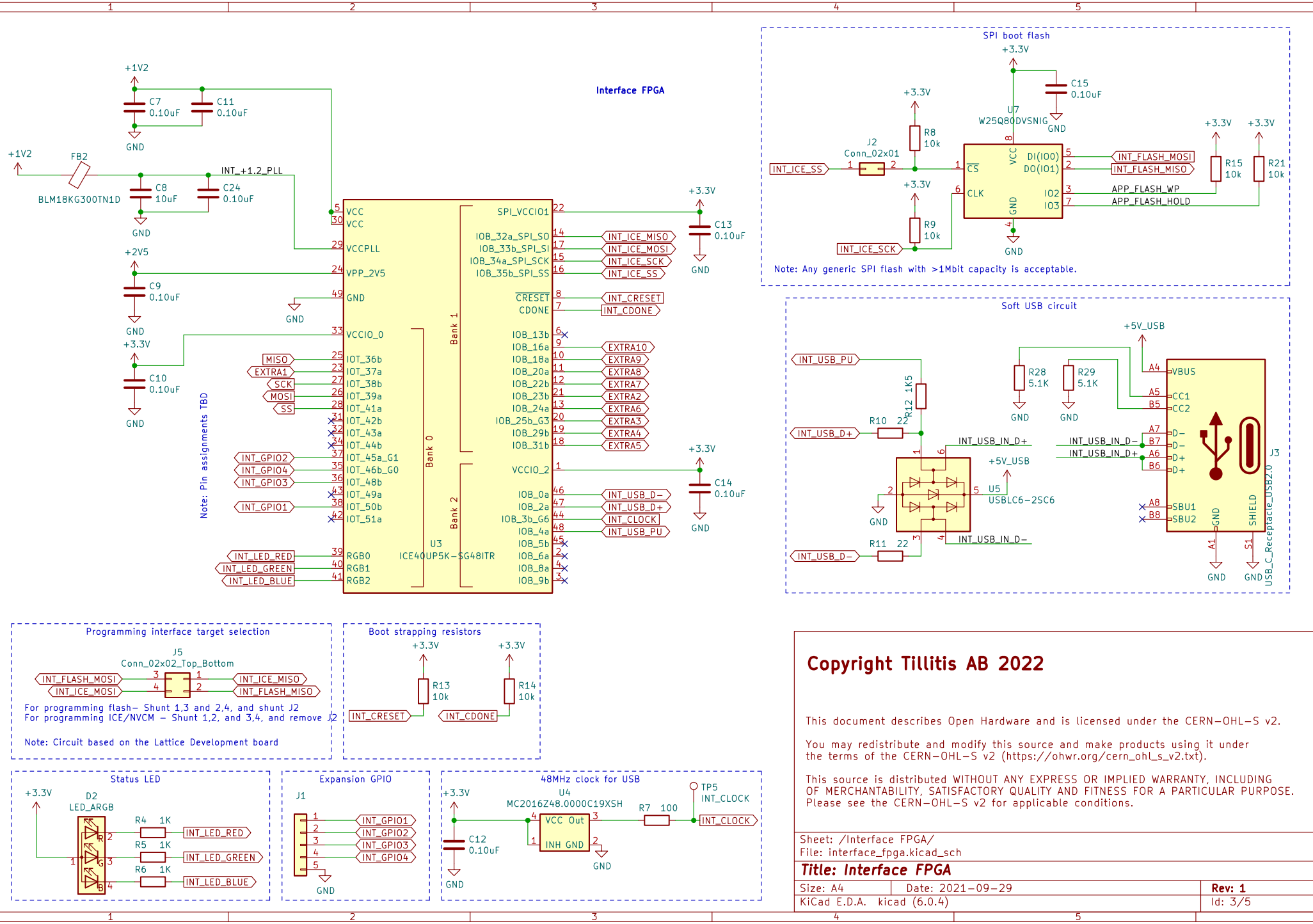
Sheet: /Application FPGA/
File: application_fpga.kicad_sch
Title: Application FPGA
Size: A4
Date: 2021–09–29
Rev: 1
KiCad E.D.A. kicad (6.0.4)
Id: 2/5


Interface FPGA
U3
ICE40UP5K-SG48ITR
Bank 0
Bank 1
Bank 2
Note: Pin assignments TBD
SPI boot flash
U7
W25Q80DVSNIG
J2
Conn_02x01
Note: Any generic SPI flash with >1Mbit capacity is acceptable.
Soft USB circuit
U5
USBLC6-2SC6
J3
USB_C_Receptacle_USB2.0
Programming interface target selection
J5
Conn_02x02_Top_Bottom
For programming flash- Shunt 1,3 and 2,4, and shunt J2
For programming ICE/NVCM - Shunt 1,2, and 3,4, and remove J2
Note: Circuit based on the Lattice Development board
Boot strapping resistors
Status LED
D2
LED_ARGB
Expansion GPIO
J1
48MHz clock for USB
U4
MC2016Z48.0000C19XSH
TP5
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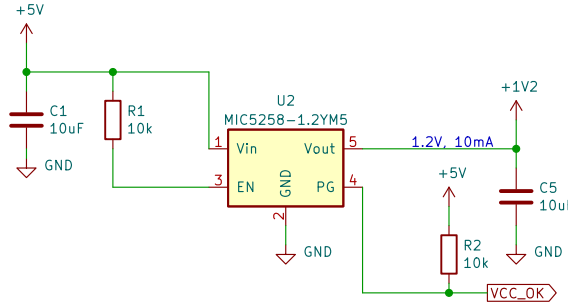
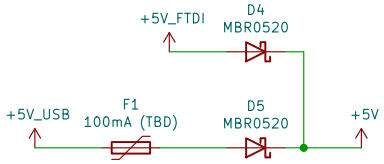
Sheet: /Interface FPGA/
File: interface_fpga.kicad_sch
Title: Interface FPGA
Size: A4
Date: 2021-09-29
Rev: 1
KiCad E.D.A. kicad (6.0.4)
Id: 3/5

1.2V regulator, supplies VCC and VCC_PLL

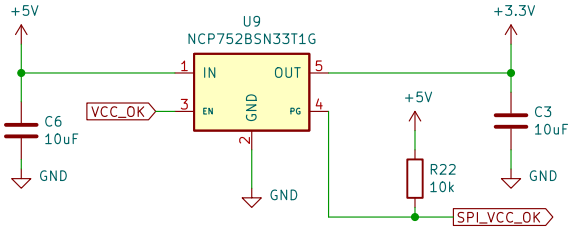


Input power selection

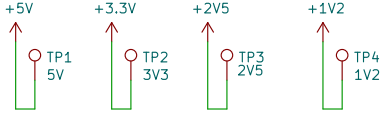


Note: Allows the board to be powered by both the interface USB and FTDI USB

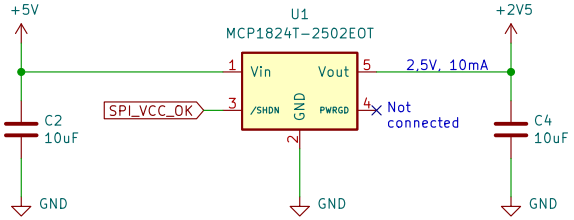
3.3V regulator, supplies VCCIO



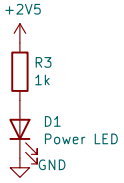
Power Supply Test Points



Regulator for 2.5V supply from 5V USB



Power LED



Note: Placed on 2.5V line, so that it shows all power rails are good

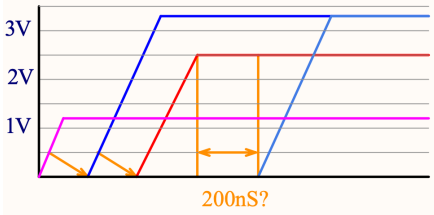
From the Lattice documentation:

4.5. Power-up Supply Sequence

It is recommended to bring up the power supplies in the following order. Note that there is no specified timing delay between the power supplies, however, there is a requirement for each supply to reach a level of 0.5 V, or higher, before any subsequent power supplies in the sequence are applied.

1. **VCC** and **VCCPLL** should be the first two supplies to be applied. Note that these two supplies can be tied together subject to the recommendation to include a RC-based noise filter on the VCCPLL. Refer to iCE40 Hardware Checklist (FPGA-TN-02006).
2. **SPI_VCCIO1** should be the next supply, and can be applied any time after the previous supplies (VCC and VCCPLL) have reached as level of 0.5 V or higher.
3. **VPP_2V5** should be the next supply, and can be applied any time after previous supplies (VCC, VCCPLL and SPI_VCCIO1) have reached a level of 0.5 V or higher.
4. **Other Supplies** (VCCIO0 and VCCIO2) do not affect device power-up functionality, and they can be applied any time after the initial power supplies (VCC and VCCPLL) have reached a level of 0.5 V or greater. There is no power down sequence required. However, when partial power supplies are powered down, it is required the above sequence to be followed when these supplies are re-powered up again.

Desired power sequence
(iCE40 UltraPlus Family Data Sheet section 4.5)



VCC, VPLL (1.2V)
SPI_VCCCIO1 (3.3V) Also VCCIO0, VCCIO2
VPP_2V5 (2.5V)
CRESET_B (internally generated)

Power-on sequence:

1. External power (3.3V_IN) is applied.
2. U2 (1.2V regulator) turns on.
3. Once 1.2V output is stable, U1 releases its PG output, allowing VCC_OK to go high.
4. U9 (3.3V regulator) turns on.
5. Once the 3.3V output is stable, U9 releases its PG output, allowing SPI_VCC_OK to go high.
6. U31(2.5V regulator) turns on.
7. After a short time, the internal POR circuit in the ICE40 allows it to boot.

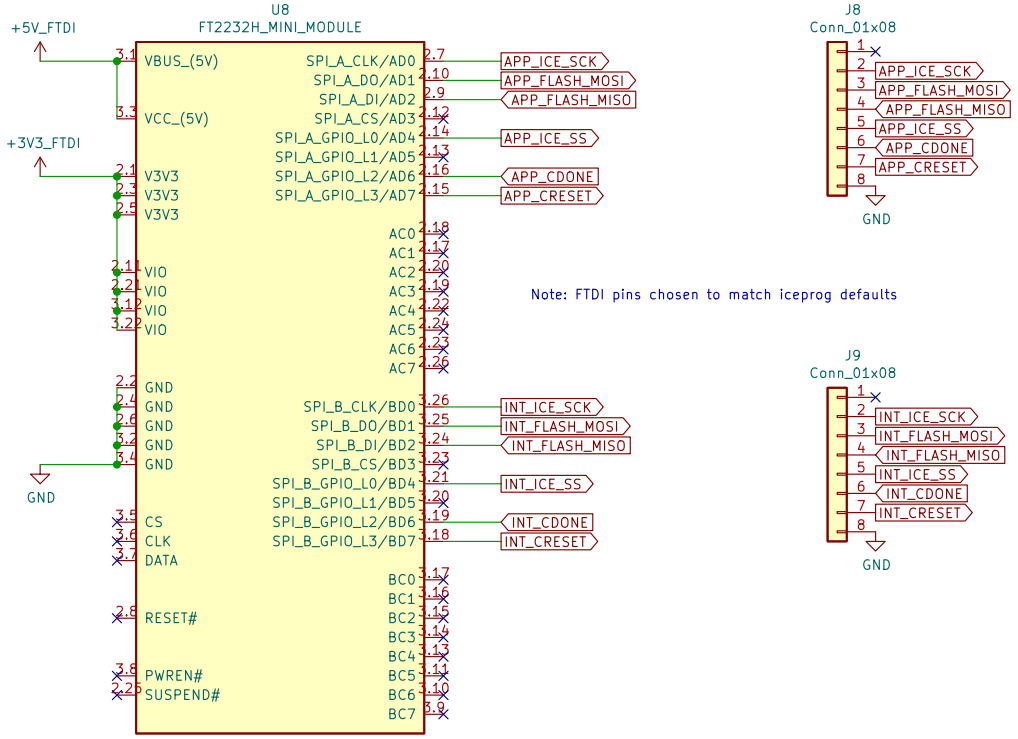
Designed by: BLIN KIN LABS

Sheet: /Power Supply/
File: powersupply.kicad_sch

Title: Power Supply

Size: A4	Date: 2021-09-29	**Rev: 1**
KiCad E.D.A. kicad (6.0.4)		Id: 4/5

FPGA programming interface



Note: FTDI pins chosen to match iceprog defaults

Sheet: /Programming Interface/
File: programming_interface.kicad_sch

Title:

Size: A4	Date: 2021-09-29	**Rev: 1**
KiCad E.D.A. kicad (6.0.4)		Id: 5/5