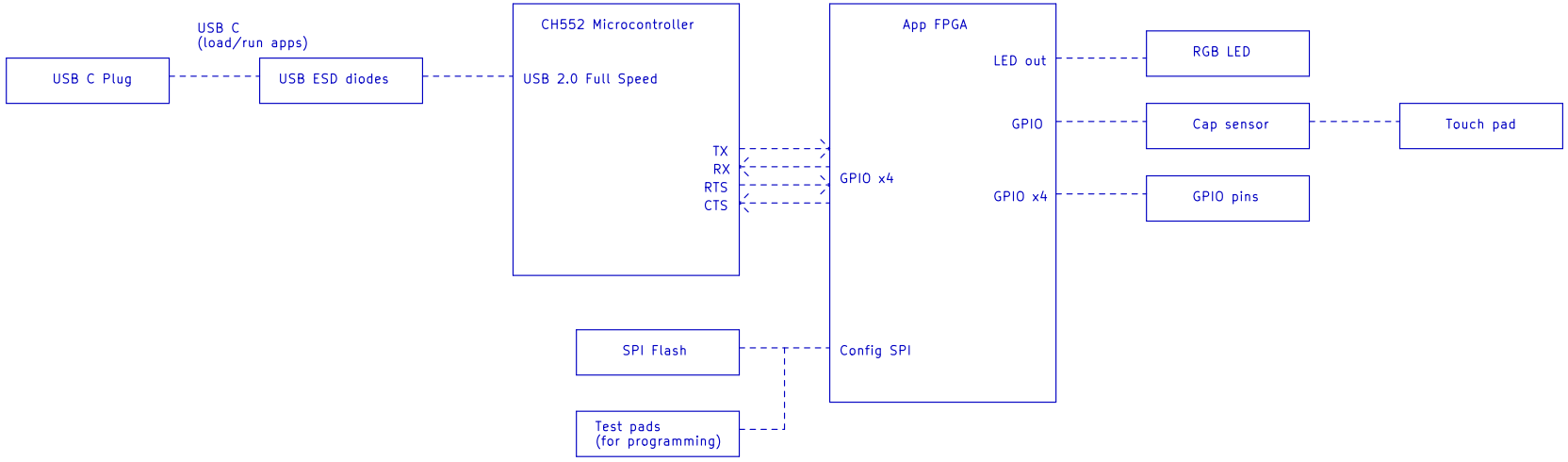
MTA1-USB-V1



3.3V LDO

2.5V LDO

1.2V LDO

Application FPGA

File: application_fpga.kicad_sch

USB to Serial converter

File: usb_to_serial.kicad_sch

Power Supply

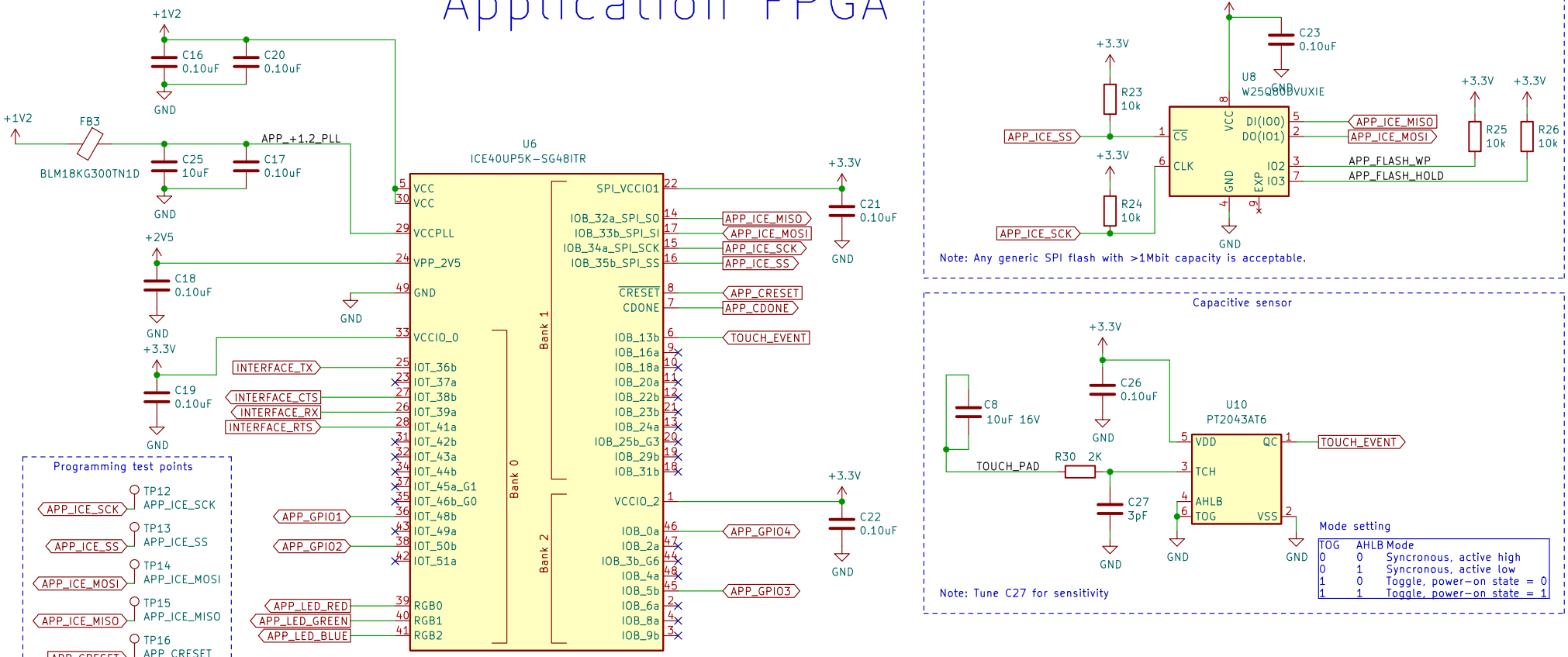
File: powersupply.kicad_sch

Sheet: /
File: mta1-usb-v1.kicad_sch

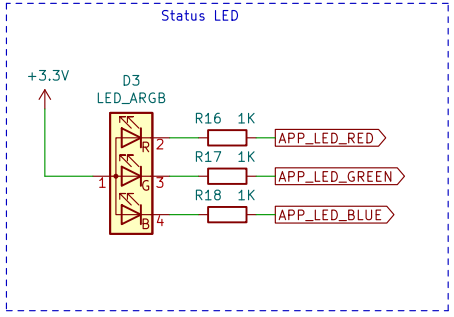
Title: MTA1-USB-V1

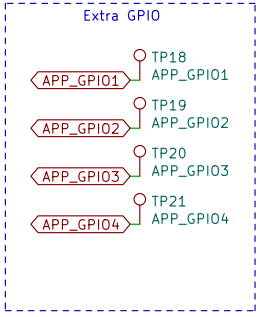
Size: A4	Date: 2021-09-29	**Rev: V1**
KiCad E.D.A. kicad (6.0.4)		Id: 1/4

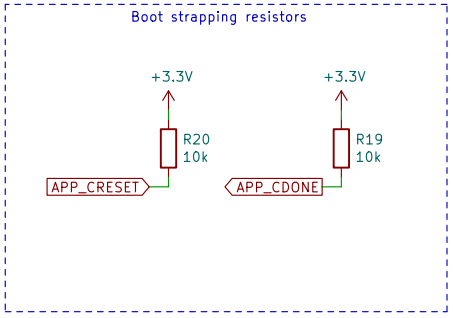
Application FPGA



FPGA signal notes:
* APP_ICE* pins are fixed and cannot be changed
* APP_LED* pins can be swapped within their group
* All other pins are generic GPIO, and can be reassigned as needed.







Mode setting

TOG	AHLB	Mode
0	0	Syncronous, active high
0	1	Syncronous, active low
1	0	Toggle, power-on state = 0
1	1	Toggle, power-on state = 1

Sheet: /Application FPGA/
File: application_fpga.kicad_sch

Title: Application FPGA

Size: A4	Date: 2021-09-29	**Rev: V1**
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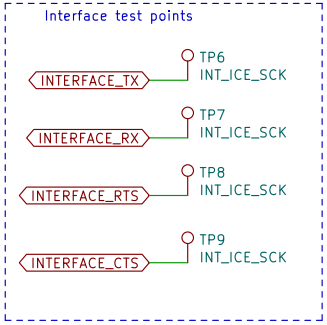
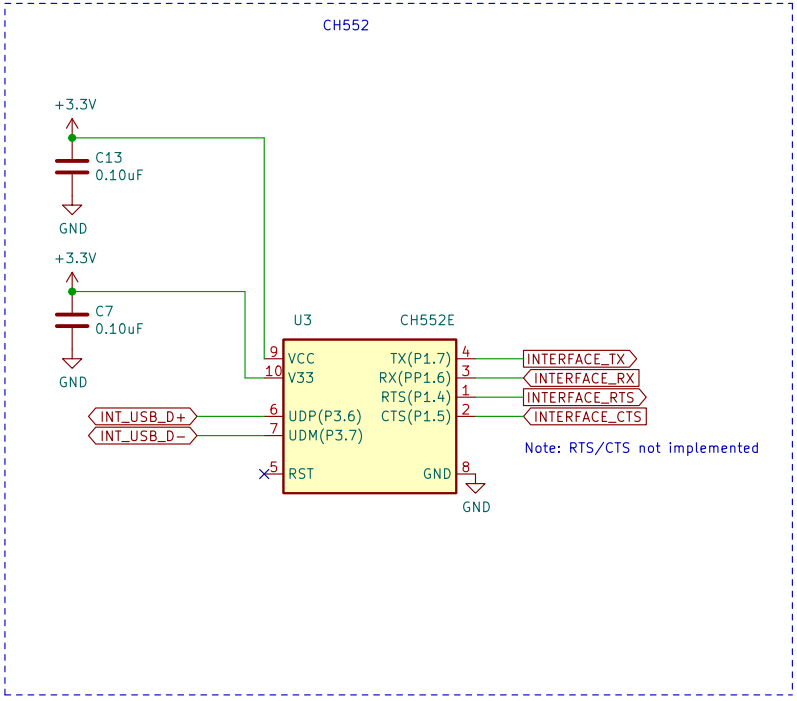
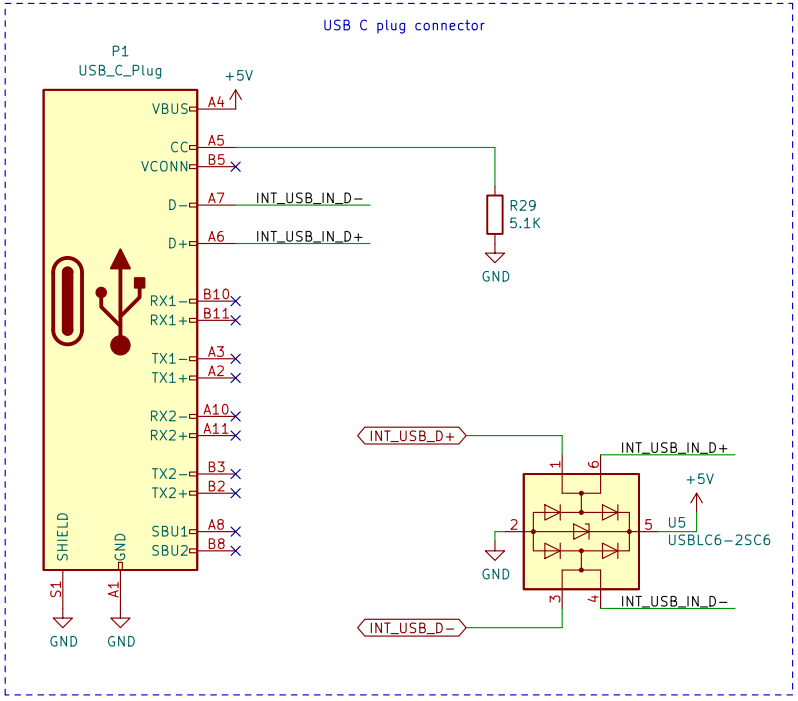
USB-to-Serial Interface







The CH552 is loaded with a TTY ACM firmware, to act as a USB-to-Serial converter

Due to the processor speed, not all baud rates are accurate. Here are the baud rates achieved for common settings:

Setting	Actual	% error
9600	9615.38	0.16%
14400	14492.75	0.64%
19200	19230.77	0.16%
38400	38461.54	0.16%
57600	58823.53	2.12%
100000	100000	0.00%
115200	125000	8.51%
128000	142857.14	11.61%
256000	333333.33	30.21%
1000000	1000000	0.00%

Note: RTS/CTS lines are not implemented in the device firmware, but are included in the hardware design in case they need to be implemented. The intent is to use them in the 'modern' sense: Each receiving device asserts it's RTS signal as long as it is able to receive at least one byte of data on it's RX line, and clears it when it is not able to receive data. Each transmitting device will check their RTS input before transmitting on their TX line.

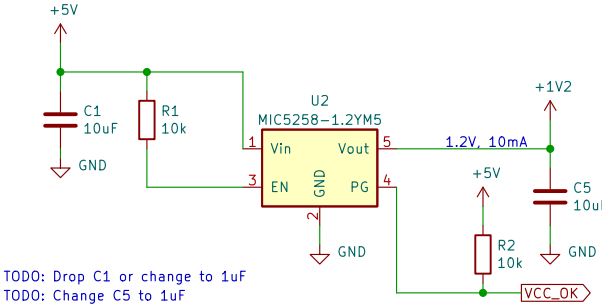
Sheet: /USB to Serial converter/
File: usb_to_serial.kicad_sch

Title: USB-to-Serial Interface

Size: A4	Date: 2021-09-29	**Rev: V1**
KiCad E.D.A. kicad (6.0.4)		Id: 3/4

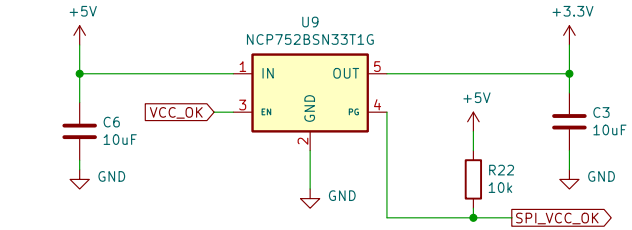
Power Supply

1.2V regulator, supplies VCC and VCC_PLL



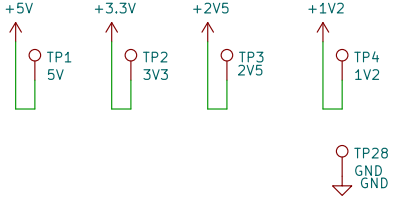
TODO: Drop C1 or change to 1uF
TODO: Change C5 to 1uF
(changes per datasheet minimum recommendations)

3.3V regulator, supplies VCCIO

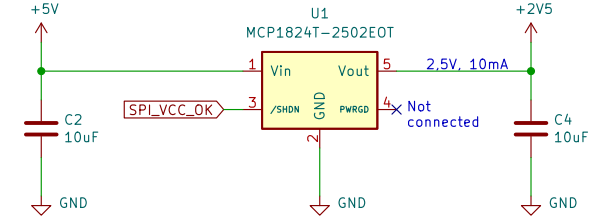


TODO: Change C6 to 1uF
TODO: Change C3 to 1uF
(changes per datasheet minimum recommendations)

Power Supply Test Points

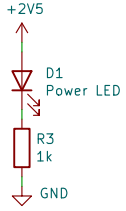


Regulator for 2.5V supply from 5V USB



TODO: Change C2 to 4.7uF
TODO: Change C4 to 1uF
(changes per datasheet minimum recommendations)

Power LED



Note: Placed on 2.5V line, so that it only lights after all voltage rails are powered.

From the Lattice documentation:

4.5. Power-up Supply Sequence

It is recommended to bring up the power supplies in the following order. Note that there is no specified timing delay between the power supplies, however, there is a requirement for each supply to reach a level of 0.5 V, or higher, before any subsequent power supplies in the sequence are applied.

1. **VCC** and **VCCPLL** should be the first two supplies to be applied. Note that these two supplies can be tied together subject to the recommendation to include a RC-based noise filter on the VCCPLL. Refer to iCE40 Hardware Checklist (FPGA-TN-02006).
2. **SPI_VCCIO1** should be the next supply, and can be applied any time after the previous supplies (VCC and VCCPLL) have reached as level of 0.5 V or higher.
3. **VPP_2V5** should be the next supply, and can be applied any time after previous supplies (VCC, VCCPLL and SPI_VCCIO1) have reached a level of 0.5 V or higher.
4. **Other Supplies** (VCCIO0 and VCCIO2) do not affect device power-up functionality, and they can be applied any time after the initial power supplies (VCC and VCCPLL) have reached a level of 0.5 V or greater. There is no power down sequence required. However, when partial power supplies are powered down, it is required the above sequence to be followed when these supplies are re-powered up again.

Power-on sequence:

1. External power (3.3V_IN) is applied.
2. U2 (1.2V regulator) turns on.
3. Once 1.2V output is stable, U1 releases its PG output, allowing VCC_OK to go high.
4. U9 (3.3V regulator) turns on.
5. Once the 3.3V output is stable, U9 releases its PG output, allowing SPI_VCC_OK to go high.
6. U31(2.5V regulator) turns on.
7. After a short time, the internal POR circuit in the ICE40 allows it to boot.

Sheet: /Power Supply/		
File: powersupply.kicad_sch		
Title: Power Supply		
Size: A4	Date: 2021-09-29	**Rev: V1**
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